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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/828,337 | 04/21/2004 | Takashi Yamada | 251383US2CONT | 5457 |

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| EXAMINER | |
|---|---|
| SOWARD, IDA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/828,337 | YAMADA ET AL. | |
| | Examiner | Art Unit | |
| | Ida M. Soward | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *29-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-48* is/are allowed.

6)☒ Claim(s) *29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed December 9, 2005.

### *Information Disclosure Statement*

The objection to the information disclosure statement has been withdrawn due to the amendment filed.

### *Specification*

The objection to the abstract of the disclosure has been withdrawn due to the amendment filed.

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 29-31 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5 of U.S. Patent No. US 6,835,981 B2 in view of Huang et al. (6,037,199).

In regard to claim 29, U.S. Patent No. US 6,835,981 B2 teaches a semiconductor chip comprising: a base substrate; a layer on a part of the base substrate, having a first device-fabrication surface in which a bulk device is positioned; a pn junction formed in the layer and positioned above an interface between the base substrate and the layer; an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; a first isolation formed in the layer so as to separate the bulk device, and a second isolation in the SOI device region so as to separate the SOI device, the first and second isolations being substantially the same depth and having a depth reaching the buried insulator; and a boundary layer located at a boundary between the layer and the SOI device region.

In regard to the layer being epitaxially grown, "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of

production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP § 2113.

In regard to claim 30, U.S. Patent No. US 6,835,981 B2 teaches the layer being a silicon layer, and the boundary layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors.

In regard to claim 31, U.S. Patent No. US 6,835,981 B2 teaches a third isolation positioned at the boundary and functioning at the boundary layer, wherein the first, second, and third isolations are of substantially the same depth.

However, U.S. Patent No. US 6,835,981 B2 fails to teach a single crystal layer.

Huang et al. teach a single crystal layer 5a (Figures 2 and 9, column 3, lines 22-27).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor chip structure as taught by U.S. Patent No. US 6,835,981 B2 with the semiconductor chip having a single crystal layer as taught by Huang et al. to increase device performance while still increasing device density (column 1, lines 13-15).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US 6,555,891 B1) in view of Huang et al. (6,037,199).

In regard to claim 29, Furukawa et al. teach a semiconductor chip 10 comprising: a base substrate 12; a layer 15 on a part of the base substrate 12, having a first device-fabrication surface in which a bulk device 50 is positioned; a pn junction (formed by 91/92 & 94) formed in the layer 15 and positioned above an interface between the base substrate 12 and the layer 15; an SOI device region 90 having a buried insulator 16 on the other part of the base substrate 12 and an SOI layer on the buried insulator 16, the SOI device region 90 having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; a first isolation 67 formed in the layer 15 so as to separate the bulk device 50, and a second isolation 68 in the SOI device region 90 so as to separate the SOI device, the first and second isolations 67 & 68 being substantially the same depth and having a depth reaching the buried insulator 16; and a boundary layer 22 located at a boundary between the layer 15 and the SOI device region 90 (Figure 11, columns 3 and 7, lines 1-26 and 6-35, respectively).

In regard to the layer being epitaxially grown, "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious

from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP § 2113.

In regard to claim 30, Furukawa et al. teach the layer 15 being a silicon layer, and the boundary layer 22 reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors (Figure 11, column 4, lines 9-15).

In regard to claim 31, Furukawa et al. teach a third isolation 65 positioned at the boundary and functioning at the boundary layer 22, wherein the first, second, and third isolations 67, 68 & 65 are of substantially the same depth (Figure 11, columns 3 and 7, lines 1-26 and 6-35, respectively).

However, Furukawa et al. fail to teach a single crystal layer.

Huang et al. teach a single crystal layer 5a (Figures 2 and 9, column 3, lines 22-27).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor chip structure as taught by Furukawa et al. with the semiconductor chip having a single crystal layer as taught by Huang et al. to increase device performance while still increasing device density (column 1, lines 13-15).

***Allowable Subject Matter***

Claims 32-48 are allowed.

### *Response to Arguments*

Applicant's arguments with respect to claims 29-31 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor chip structures:

Osanai (US 6,465,846 B1) Sun (5,399,507).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
February 20, 2006